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**Question Paper Code : 21454**

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015

Fifth Semester

Electronics and Communication Engineering

EC 2303/EC 53/10144 EC 605 — COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulations 2008/2010)

(Common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester, Electronics and Communication Engineering Regulations 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is a bus? What are the different buses in a CPU?
2. Define PC relative and Base Relative addressing mode.
3. What is pipelining and state its advantages?
4. What is Ripple-Carry Adder (RCA)?
5. Define superscalar processing.
6. What is meant by Nano programming?
7. What is translation look aside buffer?
8. Comment on locality reference.
9. What is associative memory?
10. What is bus arbitration?

PART B — (5 × 16 = 80 marks)

11. (a) Explain the following addressing modes with an example and suggest the uses of those addressing modes : (16)

- (i) Register Indirect
- (ii) Auto increment
- (iii) Indirect addressing
- (iv) Base addressing
- (v) Indexed addressing.

Or

- (b) Explain in detail about the Accumulator based CPU organization with a neat block diagram. (16)

12. (a) (i) Discuss the principle operation of carry-look ahead adders. (8)
- (ii) Discuss the non-restoring division algorithm. Simulate the same for  $8/3$ . (8)

Or

- (b) Multiply the following pair of signed nos. using Booth's bit-pair recoding of the Multiplier.

A = -8 (Multiplicand) and B = -8 (Multiplier) (16)

13. (a) Explain the hardwired and micro programmed control systems. (16)

Or

- (b) (i) Explain the pipelining and hazards. List down and brief about the types of hazards with examples. (10)
- (ii) Explain about the various branch prediction techniques. (6)

14. (a) (i) Explain in detail about the replacement policies of memory organization systems. (8)
- (ii) Give the structure of semiconductor RAM memories. Explain the read and write operations in Details. (8)

Or

- (b) Explain in detail about the cache memory organization, cache operation and address mapping. (16)

15. (a) (i) Explain in detail about the bus arbitration techniques in DMA. (8)
- (ii) Explain the short notes on vector interrupts, PCI interrupts and pipeline interrupts. (8)

Or

(b) Write short notes on :

- (i) RISC Processors (4)
- (ii) CISC Processors (4)
- (iii) Superscalar Processors (4)
- (iv) Vector Processors. (4)